

# NBXDBA012

## 3.3 V, 106.25 MHz / 212.5 MHz LVPECL Clock Oscillator

The NBXDBA012 dual frequency crystal oscillator (XO) is designed to meet today's requirements for 3.3 V LVPECL clock generation applications. The device uses a high Q fundamental crystal and Phase Lock Loop (PLL) multiplier to provide selectable 106.25 MHz or 212.5 MHz, ultra low jitter and phase noise LVPECL differential output. This device is a member of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock solutions.

Available in 5 mm x 7 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1,000.

### Features

- LVPECL Differential Output
- Uses High Q Fundamental Mode Crystal and PLL Multiplier
- Ultra Low Jitter and Phase Noise - 0.4 ps (12 kHz - 20 MHz)
- Selectable Output Frequency - 106.25 MHz (default)/ 212.5 MHz
- Total Frequency Stability -  $\pm 50$  PPM
- Hermetically Sealed Ceramic SMD Package
- RoHS Compliant
- Operating Range 3.3 V  $\pm 10\%$
- This is a Pb-Free Device

### Applications

- 1X and 2X Fiber Channel
- Host Bus Adapter

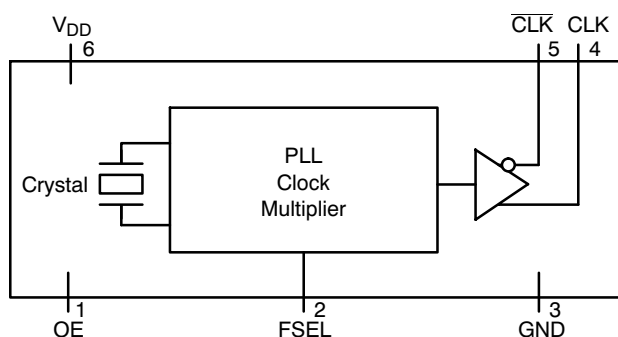
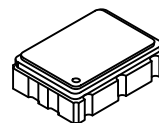


Figure 1. Simplified Logic Diagram



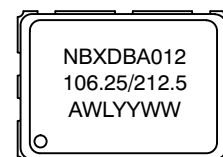
ON Semiconductor®

<http://onsemi.com>



6 PIN CLCC  
LN SUFFIX  
CASE 848AB

### MARKING DIAGRAM



NBXDBA012 = NBXDBA012 ( $\pm 50$  PPM)  
 106.25/212.5 = Output Frequency (MHz)  
 A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week

### ORDERING INFORMATION

| Device          | Package             | Shipping†        |
|-----------------|---------------------|------------------|
| NBXDBA012LN1TAG | CLCC-6<br>(Pb-Free) | 1000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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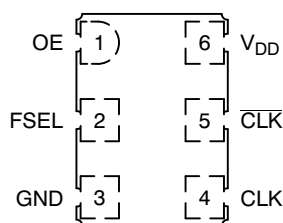


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

| Pin No. | Symbol                  | I/O                         | Description  |
|---------|-------------------------|-----------------------------|--|
| 1       | OE                      | LVTTTL/LVCMOS Control Input | Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.           |
| 2       | FSEL                    | LVTTTL/LVCMOS Control Input | Output Frequency Select Pin. Pin will default to logic HIGH when left open. See Output Frequency Select pin description Table 3. |
| 3       | GND                     | Power Supply                | Ground 0 V.  |
| 4       | CLK                     | LVPECL Output               | Non-Inverted Clock Output. Typically loaded with 50 $\Omega$ receiver termination resistor to $V_{TT} = V_{DD} - 2 V$ .          |
| 5       | $\overline{\text{CLK}}$ | LVPECL Output               | Non-Inverted Clock Output. Typically loaded with 50 $\Omega$ receiver termination resistor to $V_{TT} = V_{DD} - 2 V$ .          |
| 6       | $V_{DD}$                | Power Supply                | Positive power supply voltage. Voltage should not exceed 3.3 V $\pm 10\%$ .  |

Table 2. OUTPUT ENABLE TRI-STATE FUNCTION

| OE Pin     | Output Pins |
|------------|-------------|
| Open       | Active      |
| HIGH Level | Active      |
| LOW Level  | High Z      |

Table 3. OUTPUT FREQUENCY SELECT

| FSEL Pin                      | Output Frequency (MHz) |
|-------------------------------|------------------------|
| Open<br>(pin will float high) | 106.25                 |
| HIGH Level                    | 106.25                 |
| LOW Level                     | 212.5                  |

Table 4. ATTRIBUTES

| Characteristic   | Value                             |
|--|-----------------------------------|
| Input Default State Resistor                               | 170 k $\Omega$                    |
| ESD Protection   | Human Body Model<br>Machine Model |
|  | 2 kV<br>200 V                     |
| Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test |                                   |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

| Symbol    | Parameter                   | Condition 1         | Condition 2 | Rating      | Units              |
|-----------|-----------------------------|---------------------|-------------|-------------|--------------------|
| $V_{DD}$  | Positive Power Supply       | GND = 0 V           |             | 4.6         | V                  |
| $I_{out}$ | LVPECL Output Current       | Continuous<br>Surge |             | 25<br>50    | mA                 |
| $T_A$     | Operating Temperature Range |                     |             | -40 to +85  | $^{\circ}\text{C}$ |
| $T_{stg}$ | Storage Temperature Range   |                     |             | -55 to +120 | $^{\circ}\text{C}$ |
| $T_{sol}$ | Wave Solder                 | See Figure 8        |             | 260         | $^{\circ}\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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**Table 6. DC CHARACTERISTICS** ( $V_{DD} = 3.3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Symbol      | Characteristic                    | Conditions              | Min.                  | Typ. | Max.                  | Units         |
|-------------|-----------------------------------|-------------------------|-----------------------|------|-----------------------|---------------|
| $I_{DD}$    | Power Supply Current (Note 2)     |                         |                       | 82   | 100                   | mA            |
| $V_{IH}$    | OE and FSEL Input HIGH Voltage    |                         | 2000                  |      | $V_{DD}$              | mV            |
| $V_{IL}$    | OE and FSEL Input LOW Voltage     |                         | $GND - 300$           |      | 800                   | mV            |
| $I_{IH}$    | Input HIGH Current                | OE<br>FSEL              | -100<br>-100          |      | +100<br>+100          | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                 | OE<br>FSEL              | -100<br>-100          |      | +100<br>+100          | $\mu\text{A}$ |
| $V_{OH}$    | Output HIGH Voltage (Note 2)      | $V_{DD} = 3.3\text{ V}$ | $V_{DD}-1145$<br>2155 |      | $V_{DD}-895$<br>2405  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)       | $V_{DD} = 3.3\text{ V}$ | $V_{DD}-1945$<br>1355 |      | $V_{DD}-1600$<br>1700 | mV            |
| $V_{OUTPP}$ | Output Voltage Amplitude (Note 2) |                         |                       | 700  |                       | mV            |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Measurement taken with outputs terminated with 50 ohm to  $V_{DD}-2\text{ V}$ .

**Table 7. AC CHARACTERISTICS** ( $V_{DD} = 3.3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Symbol            | Characteristic  | Conditions                       | Min. | Typ.      | Max.     | Units  |
|-------------------|---|----------------------------------|------|-----------|----------|--------|
| $f_{CLKOUT}$      | Output Clock Frequency  | FSEL = HIGH                      |      | 106.25    |          | MHz    |
|                   |   | FSEL = LOW                       |      | 212.5     |          |        |
| $\Delta f$        | Frequency Stability - NBXDBA012   | (Note 4)                         |      |           | $\pm 50$ | ppm    |
| $\Phi_{NOISE}$    | Phase-Noise Performance<br>$f_{CLKout} = 106.25\text{ MHz}/212.5\text{ MHz}$<br>(See Figures 3 and 4) | 100 Hz of Carrier                |      | -108/-101 |          | dBc/Hz |
|                   |   | 1 kHz of Carrier                 |      | -126/-120 |          | dBc/Hz |
|                   |   | 10 kHz of Carrier                |      | -133/-126 |          | dBc/Hz |
|                   |   | 100 kHz of Carrier               |      | -133/-127 |          | dBc/Hz |
|                   |   | 1 MHz of Carrier                 |      | -140/-133 |          | dBc/Hz |
|                   |   | 10 MHz of Carrier                |      | -162/-160 |          | dBc/Hz |
| $t_{jit}(\Phi)$   | RMS Phase Jitter  | 12 kHz to 20 MHz                 |      | 0.4       | 0.9      | ps     |
| $t_{jitter}$      | Cycle to Cycle, RMS   | 1000 Cycles                      |      | 2         | 8        | ps     |
|                   | Cycle to Cycle, Peak-to-Peak  | 1000 Cycles                      |      | 12        | 30       | ps     |
|                   | Period, RMS   | 10,000 Cycles                    |      | 1         | 4        | ps     |
|                   | Period, Peak-to-Peak  | 10,000 Cycles                    |      | 8         | 20       | ps     |
| $t_{OE/OD}$       | Output Enable/Disable Time  |                                  |      |           | 200      | ns     |
| $t_{DUTY\_CYCLE}$ | Output Clock Duty Cycle<br>(Measured at Cross Point)  |                                  | 48   | 50        | 52       | %      |
| $t_R$             | Output Rise Time (20% and 80%)  | (See Figures 5 and 6)            |      | 250       | 400      | ps     |
| $t_F$             | Output Fall Time (80% and 20%)  | (See Figures 5 and 6)            |      | 250       | 400      | ps     |
| $t_{start}$       | Start-up Time   |                                  |      | 1         | 5        | ms     |
|                   | Aging   | 1 <sup>st</sup> Year             |      |           | 3        | ppm    |
|                   |   | Every Year After 1 <sup>st</sup> |      |           | 1        | ppm    |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

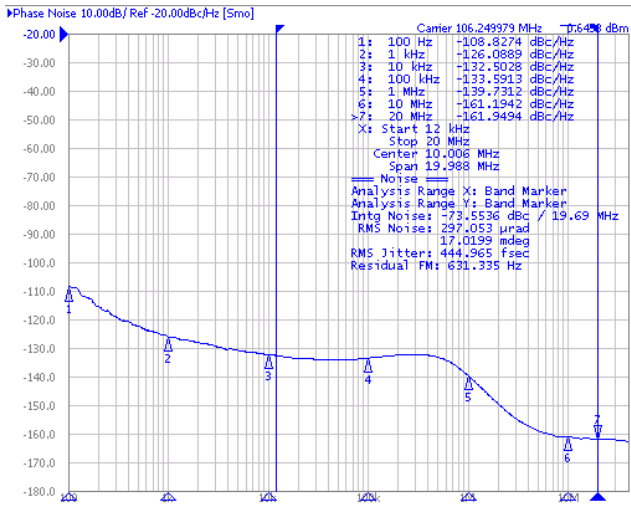
3. Measurement taken with outputs terminated with 50 ohm to  $V_{DD}-2\text{ V}$ . See Figure 7.

4. Parameter guarantees 10 years of aging. Includes initial stability at  $25^\circ\text{C}$ , shock, vibration, and first year aging.

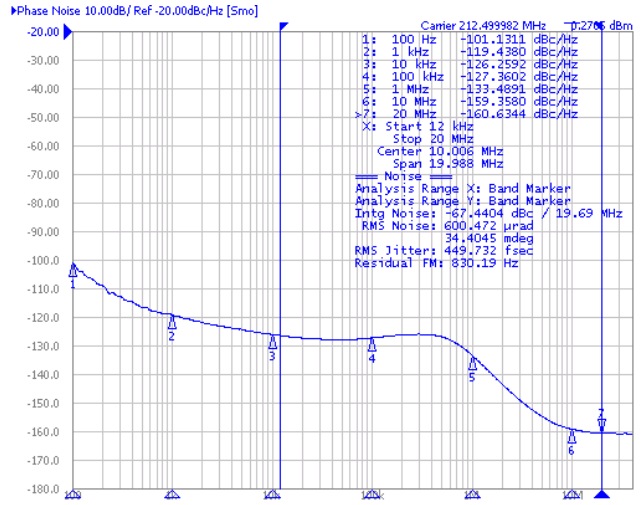
# NBXDBA012

**Table 8. RELIABILITY COMPLIANCE**

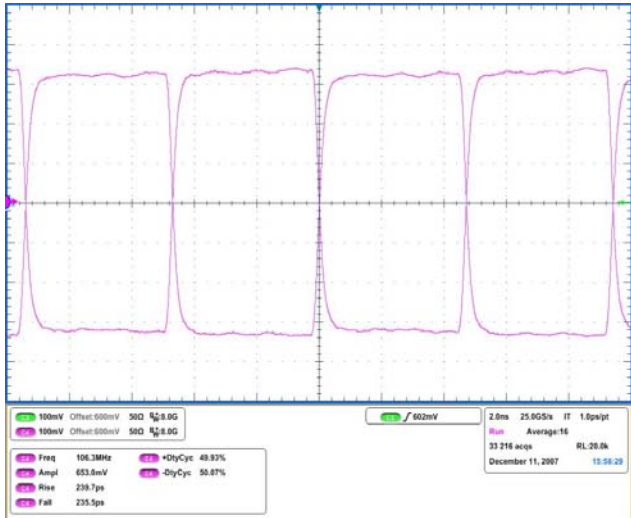
| Parameter                  | Standard    | Method                                |
|----------------------------|-------------|---------------------------------------|
| Shock                      | Mechanical  | MIL-STD-833, Method 2002, Condition B |
| Solderability              | Mechanical  | MIL-STD-833, Method 2003              |
| Vibration                  | Mechanical  | MIL-STD-833, Method 2007, Condition A |
| Solvent Resistance         | Mechanical  | MIL-STD-202, Method 215               |
| Thermal Shock              | Environment | MIL-STD-833, Method 1011, Condition A |
| Moisture Level Sensitivity | Environment | MSL1 260°C per IPC/JEDEC J-STD-020D   |



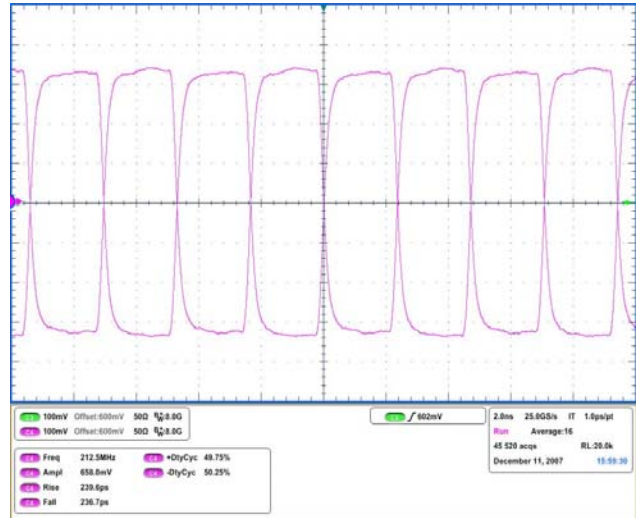
**Figure 3. Typical Phase Noise Plot @ 106.25 MHz**



**Figure 4. Typical Phase Noise Plot @ 212.5 MHz**

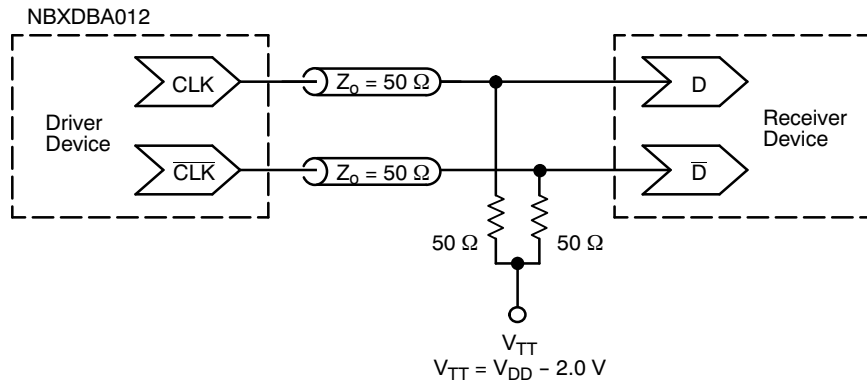


**Figure 5. Typical Output Waveform @ 106.25 MHz**

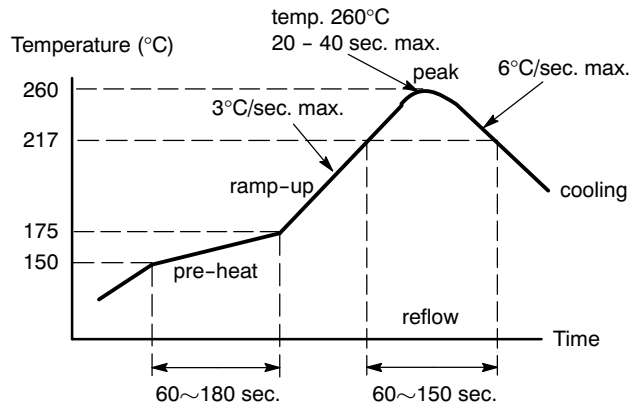


**Figure 6. Typical Output Waveform @ 212.5 MHz**

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**Figure 7. Typical Termination for Output Driver and Device Evaluation**  
 (See Application Note AND8020/D – Termination of ECL Logic Devices.)

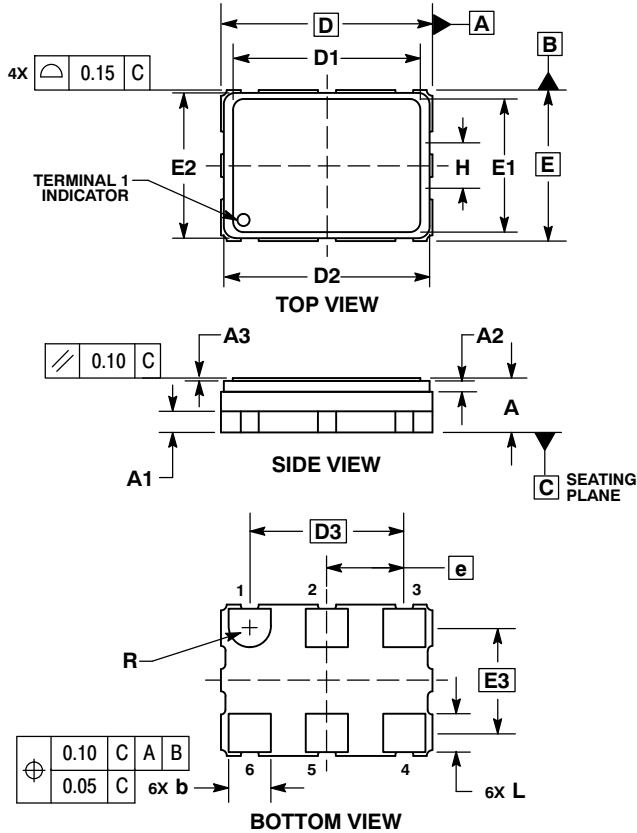


**Figure 8. Recommended Reflow Soldering Profile**

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## PACKAGE DIMENSIONS

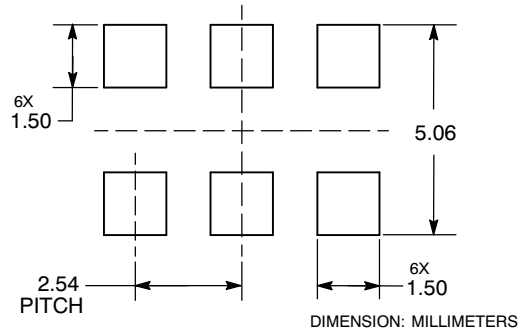
6 PIN CLCC, 7x5, 2.54P  
CASE 848AB-01  
ISSUE C



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.  
 2. CONTROLLING DIMENSION: MILLIMETERS.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | NOM  | MAX  |
| A   | 1.70        | 1.80 | 1.90 |
| A1  | 0.70 REF    |      |      |
| A2  | 0.36 REF    |      |      |
| A3  | 0.08        | 0.10 | 0.12 |
| b   | 1.30        | 1.40 | 1.50 |
| D   | 7.00 BSC    |      |      |
| D1  | 6.17        | 6.20 | 6.23 |
| D2  | 6.66        | 6.81 | 6.96 |
| D3  | 5.08 BSC    |      |      |
| E   | 5.00 BSC    |      |      |
| E1  | 4.37        | 4.40 | 4.43 |
| E2  | 4.65        | 4.80 | 4.95 |
| E3  | 3.49 BSC    |      |      |
| e   | 2.54 BSC    |      |      |
| L   | 1.17        | 1.27 | 1.37 |
| R   | 0.70 REF    |      |      |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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